PhD Qualifying Exam on Architecture
May 2008
Department of Computer Science
Georgia State University

Put an X through the question numbers that you do not answer.

Question
1
2
3
4
5
6

Note: You are only required to answer five questions out of the six questions given below. **Do not** answer more than five questions. On the front page, put an X in the score area of the questions that you skip. On upper RIGHT corner of each answer sheet, write "Question # ___". On lower RIGHT corner of each answer sheet, write "Page # ___". Make sure pages are in order. Make sure to show your work to ensure partial credit.

1. A two-way set associative cache memory uses blocks of eight words. The cache can accommodate a total of 2048 words from main memory. The main memory size is 128K x 32.

   (a) Formulate all pertinent information required to construct the cache memory. Draw a diagram of the cache organization with all the information.

   (b) What is the size of the cache memory?

   (c) Explain the major difference between direct mapping cache and set-associative mapping cache.

   (d) How does a data cache take advantage of spatial locality? Give one example.

2. The basic computer instructions for the model computer are listed in the following table (Figure 1), from Manos textbook.

Insert here table 6.1 from Mano's Computer System Architecture book.

Figure 1: figure

   (a) Explain in words what the following program accomplishes when it is executed.

   (b) What is the value of location TMP during the execution of the program?

   (c) Explain in words how to optimize the program in terms of computing efficiency.

```
        ORG  100
        CLE
        CLA
        STA  TMP
        LDA  WRD
        SZA
        BUN  ROT
        BUN  STP

ROT,    CIL
        SZE
        BUN  AGN
        BUN  ROT

AGN,    CLE
        ISZ  TMP
        SZA
        BUN  ROT
        LDA  TMP   /(1), TMP=_________
        CMA
        INC
        STA  TMP
        CLA
```

```
LOP,    ADD  B
        ISZ  TMP
        BUN  LOP

STP,    HLT         /(2), TMP=_________

TMP,    HEX  0

WRD,    HEX  42C0

B,      DEC  5
        END
```

3. Pipeline speedup is given by the following equation:

$$S = \frac{nt_n}{(k+n-1)t_p}$$

where n is the number of instructions, t_n is the time to complete each instruction (of a non-pipelined system) and t_p is the clock cycle time for a pipeline of k segments.

Suppose we have System A: a non-pipelined system that need 30 ns to complete a instruction, and System B: a system with 5 pipeline stages.

   (a) If the pipeline segments take 10, 8, 12, 15, and 11 ns to complete their work, what is t_p? Explain your answer.

   (b) How long will each system take to compute 10, 50, 100, and 10,000 instructions? (Assume there are no branches.)

   (c) What is the speedup for 10, 50, 100, and 10,000 instructions? (Assume there are no branches.)

   (d) If there were branches, how would this affect your answers above?

4. Figure 2 shows an example 4-bit circuit. Examining the inputs and outputs, what arithmetic operations does it perform? What logical operations does it perform? Explain, including any truth-tables or diagrams to support your answer. Suppose we also have inputs D_0, D_1, D_2, and D_3. Show how we could add to this circuit to provide a choice between outputting the G outputs or the D signals.

Insert here figure 10.5 from Mano and Kime's book.

Figure 2: Logic Diagram

5. The mapping procedure is used to relate instructions to the corresponding micro routine located in the control memory.

   (a) The basic computer contains six basic instructions, shown in Table 1. Append Table 6 with the needed 20 bit binary codes for all micro instructions. Use the mapping procedure to get all addresses. (Also see tables 6, 2, 3, 4 and 5.)

   (b) Explain how the following operation can be performed by listing all needed instructions using instructions from Table 1 only.
   AC $\leftarrow$ [AC $\wedge$ M(EA)]

6. The following arithmetic function, F, is used to evaluate an input X, $F = (X^2 + X + 11)_5$, where X is an unsigned integer number stored in 3 bit register.

   (a) Indicate the most economical size in bits of the register needed to store the result of F without overflow?

   (b) Construct the truth table for F listing all input and output bits

   (c) Minimize each output with respect to inputs in sum of products and product of sums.

   (d) Use the most economical multiplexer to design the circuit.

   (e) Use the most economical decoder to design the same circuit.

Insert here figure 7.5 from Mano's Computer System Architecture book.

Symbol	Opcode	RTL
OR	0100	AC ← AC ∨ M(EA)
COMPLEMENT	0101	AC'

Table 1: From Mano's Architecture Book

Insert here table 7.1 from Mano's Computer System Architecture book.

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Table 2: From Mano's Architecture Book

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Table 3: From Mano's Architecture Book

Insert here table 7.1 from Mano's Computer System Architecture book.

Table 4: From Mano's Architecture Book

Insert here table 7.1 from Mano's Computer System Architecture book.

Table 5: From Mano's Architecture Book

Insert here table 7.3 from Mano's Computer System Architecture book.

Table 6: control memory contents

Table 7: table